## CV2xx Series Printed Wiring Board Design Guidelines

## Introduction

WJ Communications has developed a line of dual-branch converters designed for mobile infrastructure applications (CV210-1, CV210-2, CV210-3, CV211-1, CV211-2, CV211-3, collectively referred to as CV2xx). These converters provide two RF to IF conversion branches driven by a common LO amplifier, and are intended to serve the primary and diversity receive chains for a single- or multicarrier transceiver card. The converters provide a significant reduction in cost, design complexity, and board size vs. implementation as discrete components. However, certain key application circuit elements are important to achieve optimal performance. In this note, two application circuits (CV210-3 and CV211-1) intended for the use with the CV2xx product series are described in detail. Application circuits for the other CV2xx models are similar with their BOM's listed in Appendix 2. More information regarding their application circuits are shown in their respective datasheets.

Generic functional block diagrams for the converters and essential external circuitry are shown in Figures 1 and 2, for the cellular and PCS / UMTS application circuits respectively. The green shaded areas represent the converter and the red shaded areas are the required support circuitry. Bias circuitry for the amplifiers is also required, but is not shown here for clarity; bias circuits will be discussed below in connection with the detailed circuit schematics.

The cellular-band converters require an external diplexer that is incorporated in the application circuit because implementing an on-chip diplexer at this low frequency consumes significant semiconductor area. The PCS-band and UMTS-band converters utilize a diplexer that is incorporated on chip. All of the CV2xx converter application circuits include IF matching circuits to optimize IF amplifier performance over the IF band of interest.


Figure 1: Cellular dual-branch converter block diagram.


Figure 2: PCS/UMTS dual-branch converter block diagram.

## Application Printed Wiring Board

The CV2xx converters are designed in 28-pin QFN surfacemount packages. A single application PWB has been designed for the dual branch converter product line. This PWB can be used for either the cellular or PCS/UMTS bands. By simply using $0 \Omega$ jumpers or 'no-loading' components the PWB can be tailored to the RF and IF bands of interest. The main layout consideration is keeping the external diplexer components in close proximity to the QFN package. Files of the latest revision of the dual branch converter PWB layout will be available from the WJ Communications web site (www.wj.com) in AutoCAD 'dwg' or 'dxf' format as a guide for user PWB design. Figure 3 shows the dual branch converter application PWB.


Figure 3: Current revision of the dual branch converter PWB.

## Application Circuit Card Assembly

Connectorized circuit card assemblies (CCA's) populated with dual-branch converters and required discrete components are available for qualified customers to evaluate the performance of the converters. Sample requests may be submitted through the website or through worldwide sales and distribution. Figure 4 below shows an assembled CCA.


Figure 4: Fully assembled CV211-2 Sample Evaluation Board.

## Application Board Configuration

CV210-3: Figure 5 shows the application circuit for the cellular band CV210-3 with an IF center frequency of 240 MHz . The application circuit can be broken up into four functions: diplexing, IF amplifier matching, IF lowpass filtering, and dc biasing.

Diplexer: In a downconversion application, the incoming RF signal impinges on the switching elements of the mixer; the interaction with these switches produces a signal at the IF frequency. The two signals (RF and IF) are directed to the appropriate ports by the external diplexer. The CV210-3 uses a four-element diplexer at an IF of 240 MHz . Figure 5 shows the component values for the four element diplexer with $0 \Omega$ jumpers for C16, C17, L10 and, L11. A six-element diplexer circuit, utilizing C16, C17, L10, and L1 is required for the CV210-3 when IF frequencies greater than 300 MHz are desired.

One may notice that there are transmission lines shown to pins 1 and 7. These transmission lines are required for PCS/UMTS applications and have no function when used with a cellular converter, which has no internal connection to pins 1 and 7.

IF amplifier match: The IF amplifier requires matching elements to optimize the performance of the amplifier to the desired IF center frequency. Since IF bandwidths are typically on the order of 5 to $10 \%$, a simple two element matching network, in the form of either a high-pass or low-pass filter structure, is sufficient to match the MMIC IF amplifiers over these narrow bandwidths. For larger IF bandwidth requirements, a four element matching network may be employed.

The current WJ application board makes use of the low-pass structure for two reasons. The first reason is that a low-pass structure helps the CVxxx's L-I isolation, and second reason is that tests performed by WJ shows better NF when using the lowpass configuration. S-parameters for the IF amplifier in the QFN package will soon be made available on the website so users may design their own matching topologies. Appendix 2 lists the required component values for various different IF center frequencies. These values may be used on any of the dual-branch application circuits to center the IF amplifier match, provided that the IF frequency is within the specification limits of the downconverter.

IF lowpass filter: Filtering of unwanted RF and LO signals are typically performed in the IF chain. This filtering function may be realized using lumped elements, distributed elements or SAW devices. Placeholders (C21, C22, C23, C24, L12, and L13, all marked ' XXX ' or ' 0 ') are provided in the application circuit to allow for lumped-element filtering to be implemented if desired.

DC biasing: DC bias must be provided for the LO and IF amplifiers in the converter. One of the key issues in designing the bias network is the choice of a value for R1, which sets operating current for the last stage of the LO amplifier and is chosen to optimize the mixer LO drive level. As this resistor value is increased, the LO drive to the mixer will decrease, causing the mixer Input IP3 to decrease. As the resistor is decreased, LO drive will increase and cause conversion gain to decrease. The choice of resistor must also be consistent with the maximum allowable current for the output stage of the LO amplifier, which cannot exceed 120 mA at any operating condition to ensure long-term reliability. For the CV210-3, a value of $10 \Omega$ is optimal.

The IF amplifier bias circuit requires an RF choke. Our application circuit uses a wire-wound 220 nH inductor of size 0805. The inductor needs to be sized as an 0805 to deal with the power dissipation in this component; the value is chosen to optimize the IF output return loss.

CV211-1: Figure 6 shows the application circuit for the PCS/UMTS band CV211-1 with an IF center frequency of 240 MHz . Since the PCS/UMTS products have an internal diplex function, no external diplexer is required. In this case, pins 1 and 7 are active and provide the RF input path. Therefore, components C2, C3, C6, C8, C16, C17, L2, and L6 should be either no loaded or omitted from the layout. L3, L7, L10, and L11 can also be $\Omega \Omega$ jumpers or replaced with short lengths of transmission lines. Also please note that the value for R1 for optimum LO drive level is $11 \Omega$ for the CV211-1.

## Summary

With proper design techniques, the WJ dual-branch converters can be optimized for an IF frequency within the product's specification window. Two specific examples for a cellular-band downconverter and a PCS-band downconverter were covered in this application note. The same techniques can be applied to the other models. WJ Application Engineers are available by email (applications.engineering @ wj.com) or by phone (800-876-6093) if further assistance is required.


Figure 5. Schematic for the CV210-3 with an IF center frequency of 240 MHz


Figure 6. Schematic for the CV211-1 with an IF center frequency of 240 MHz

## Appendix 1: Bill of Materials for CV2xx Application Circuits

CV210-1PCB75 Bill of Materials
IF $=70 \mathrm{MHz}$

| Ref. Desig. | Component |
| :--- | :--- |
| R1 | $11.3 \Omega$ chip resistor, <br> size 0805 |
| R2, R3, R4 <br> R4, L10, L11 <br> L12, L13, C16 <br> C17 | $0 \Omega$ chip resistor |
| R6, R7 | $3.3 \Omega$ chip resistor |
| L1 | 120 nH chip inductor |
| L2, L6 | 12 nH chip inductor |
| L3, L7 | 22 nH chip inductor |
| L4, L8 | 150 nH chip inductor |
| L5, L9 | 220 nH chip inductor <br> size 0805 |
| C1, C5, C10 <br> C15 | 1000 pF chip capacitor |
| C2, C8 | 3.9 pF chip capacitor |
| C3, C9 | 8.2 pF chip capacitor |
| C4, C11 | 22 pF chip capacitor |
| C6, C12, C14 | $.01 \mu \mathrm{~F}$ chip capacitor |
| C7, C13 | 100 pF chip capacitor |
| C18, C19, C20 <br> C21, C22, C23 | DNP |
| C24 |  |

CV211-1PCB240 Bill of Materials
IF $=240 \mathrm{MHz}$

| Ref. Desig. | Component |
| :--- | :--- |
| R1 | $13 \Omega$ chip resistor, <br> size 0805 |
| R2, R3, R4 <br> R4, L3, L7 <br> L10, L11, L12 <br> L13, C16, C17 | $0 \Omega$ chip resistor |
| R6, R7 | $2.2 \Omega$ chip resistor |
| L1 | 120 nH chip inductor |
| L3, L7 | 22 nH chip inductor |
| L4, L8 | 56 nH chip inductor |
| L5, L9 | 220 nH chip inductor <br> size 0805 |
| C1, C5, C10 <br> C15 | 1000 pF chip capacitor |
| C4, C11 | 2 pF chip capacitor |
| C6, C12, C14 | $.01 \mu$ F chip capacitor |
| C7, C13 | 100 pF chip capacitor |
| L2, L6, C2, C3 <br> C8, C9, C16 C17, <br> C18, C19 C20, <br> C21, C22 C23, <br> C24 | DNP |
| D1 | Jumper wire <br> (or 0 $\Omega$ resistor) |
| U1 | CV211-1 WJ Converter |

CV210-2PCB240 Bill of Materials
IF $=240 \mathrm{MHz}$

| Ref. Desig. | Component |
| :--- | :--- |
| R1 | $11.3 \Omega$ chip resistor, <br> size 0805 |
| R2, R3, R4 <br> R4, L12, L13 | $0 \Omega$ chip resistor |
| R6, R7 | $2.2 \Omega$ chip resistor |
| L1 | 120 nH chip inductor |
| L2, L6 | 12 nH chip inductor |
| L3, L7 | 33 nH chip inductor |
| L4, L8 | 56 nH chip inductor |
| L5, L9 | 220 nH chip inductor <br> size 0805 |
| L10, L11 | 15 nH chip inductor |
| C1, C5, C10 <br> C15 | 1000 pF chip capacitor |
| C2, C8 | 5.6 pF chip capacitor |
| C3, C9 | 8.2 pF chip capacitor |
| C4, C11 | 2 pF chip capacitor |
| C6, C12, C14 | $.01 \mu$ chip capacitor |
| C7, C13 | 100 pF chip capacitor |
| C16, C17 | 8.2 pF chip capacitor |
| C18, C19, C20 <br> C21, C22, C23 <br> C24 | DNP |
| D1 | Jumper wire <br> $($ or $0 \Omega$ resistor $)$ |
| U1 | CV210-2 WJ Converter |

CV211-2PCB240 Bill of Materials
IF $=240 \mathrm{MHz}$

| Ref. Desig. | Component |
| :--- | :--- |
| R1 | $13 \Omega$ chip resistor, <br> size 0805 |
| R2, R3, R4 <br> R4, L3, L7 <br> L10, L11, L12 <br> L13, C16, C17 | $0 \Omega$ chip resistor |
| R6, R7 | $2.2 \Omega$ chip resistor |
| L1 | 120 nH chip inductor |
| L3, L7 | 22 nH chip inductor |
| L4, L8 | 56 nH chip inductor |
| L5, L9 | 220 nH chip inductor |
| size 0805 |  |

CV210-3PCB240 Bill of Materials
IF $=\mathbf{2 4 0} \mathbf{~ M H z}$

| Ref. Desig. | Component |
| :--- | :--- |
| R1 | $11.3 \Omega$ chip resistor, <br> size 0805 |
| R2, R3, R4 <br> R4, L10, L11 <br> L12, L13, C16 <br> C17 | $0 \Omega$ chip resistor |
| R6, R7 | $2.2 \Omega$ chip resistor |
| L1 | 120 nH chip inductor |
| L2, L6 | 12 nH chip inductor |
| L3, L7 | 22 nH chip inductor |
| L4, L8 | 56 nH chip inductor |
| L5, L9 | 220 nH chip inductor <br> size 0805 |
| C1, C5, C10 <br> C15 | 1000 pF chip capacitor |
| C2, C8 | 3.9 pF chip capacitor |
| C3, C9 | 8.2 pF chip capacitor |
| C4, C11 | 2 pF chip capacitor |
| C6, C12, C14 | $.01 \mu \mathrm{~F}$ chip capacitor |
| C7, C13 | 100 pF chip capacitor |
| C18, C19, C20 <br> C21, C22, C23 | DNP |
| C24 | Jumper wire <br> (or $0 \Omega$ resistor) |
| D1 | CV210-3 WJ Converter |
| U1 |  |

## CV211-3PCB75 Bill of Materials

IF $=70 \mathrm{MHz}$

| Ref. Desig. | Component |
| :--- | :--- |
| R1 | $13 \Omega$ chip resistor, <br> size 0805 |
| R2, R3, R4 <br> R4, L3, L7 <br> L10, L11, L12 <br> L13, C16, C17 | $0 \Omega$ chip resistor |
| R6, R7 | $3.3 \Omega$ chip resistor |
| L1 | 120 nH chip inductor |
| L3, L7 | 22 nH chip inductor |
| L4, L8 | 150 nH chip inductor |
| L5, L9 | 220 nH chip inductor <br> size 0805 |
| C1, C5, C10 <br> C15 | 1000 pF chip capacitor |
| C4, C11 | 22 pF chip capacitor |
| C6, C12, C14 | $.01 \mu \mathrm{~F}$ chip capacitor |
| C7, C13 | 100 pF chip capacitor |
| L2, L6, C2, C3 <br> C8, C9, C16 C17, | DNP |
| C18, C19 C20, | D21, C22 C23, |

All components are of size 0603 unless otherwise specified. DNP represents "Do Not Place.

## Appendix 2: Recommended Component Values for Various IF Center Frequencies

| Ref. Desig. | Component Value |  |  |
| :---: | :---: | :---: | :---: |
|  | $\mathbf{I F}=\mathbf{7 0} \mathbf{~ M H z}$ | $\mathbf{I F}=\mathbf{1 7 0} \mathbf{M H z}$ | $\mathbf{I F}=\mathbf{2 4 0} \mathbf{~ M H z}$ |
| R6, R7 | 3.3 | 2.2 | 2.2 |
| L4, L8 | 150 | 82 | 56 |
| L5, L9 | 220 | 220 | 220 |
| C4, C11 | 22 | 4.7 | 2.0 |

